What is Claimed is:

1. A method of manufacturing a flash memory device, the method comprising the steps of;

(a) providing a semiconductor substrate having a high voltage transistor area in which a first gate oxide film and a first poly-silicon layer are formed between first element isolation films, and a low voltage transistor/cell area in which a second gate oxide film and the first poly-silicon layer are formed between second element isolation films;

(b) forming a planarizing film on the surfaces of the first poly-silicon layer and the first and second element isolation films;

(c) performing a first etching process to remove upper portions of the planarizing film and the element isolation films in the low voltage transistor/cell area to a certain thickness;

(d) performing a second etching process to remove upper portions of the planarizing film and the element isolation films in the high voltage transistor area and the low voltage transistor/cell area; and,

(e) forming a second poly-silicon layer on the surfaces of the first poly-silicon layer and the element isolation films.

2. The method of claim **1**, wherein the planarizing film is formed by using an SOG or a BPSG to have a thickness in the range of about 300 Å to about 800 Å.

3. The method of claim **1**, further comprising the step of forming a buffer oxide film between the first poly-silicon layer and the planarizing film.

4. The method of claim **3**, wherein the buffer oxide film has a thickness in the range of about 20 Å to about 100 Å.

5. The method of claim **1**, wherein the first and second etching processes comprise a wet etching process using an oxide etching solution with HF added.

6. The method of claim **1**, further comprising forming, prior to step (c), a photo resist pattern to close the high voltage transistor area and open the low voltage transistor/cell area.

7. The method of claim **6**, further comprising removing the photo resist pattern by a wet or dry etching after the first etching process is completed.

8. The method of claim **1**, further comprising performing the first and second etching processes to obtain an oxide height (EFH) in the high voltage transistor area and the low voltage transistor/cell area of about (-) 100 Å to about 50 Å.